Symbol and Channel Assignment Tables

This section lists the symbol tables, channel assignment tables for disassembly and timing, and signal acquisition for each of the support packages.

Symbol Tables

The TCS101 product supplies three symbol table files for the SPI3_TX and SPI3_RX supports and one each for SPI4 and SPI4_LVTTL support packages.

Tables 3–4 through 3–10 show the definitions for the symbol, bit pattern, and meaning of the group symbols in the control symbol tables. The symbol table file for SPI3_TX support package is SPI3_TX_Ctrl.

Table 3–4: SPI3_TX_Ctrl group symbol table definitions

Symbol	Ctrl group value TSX TENB TSOP TEOP TERR TPRTY TMOD1 TMOD0	Description
DATA	0 0 0 0 X X X X	Valid data on TDAT bus
EOP	0 0 0 1 0 X X X	Sample at which TEOP is asserted
SOP	0 0 1 0 X X X X	Sample at which TSOP is asserted
ERROR	0 0 X 1 1 X X X	Erroneous packet transmitted over TDAT bus
PORT_ADDRESS	1 1 0 0 X X X X	Physical port address
SOP&EOP	X 0 1 1 X X X X	Sample at which TSOP and TEOP are asserted

***NOTE**. Binary values are displayed for those control group words that do not have any symbols assigned to them.*

Table 3–5 shows the definitions for the symbol, bit pattern, and meaning of the group symbols in the EasyTrigger symbol table for the SPI3_TX support package. The EasyTrigger symbol table file name SPI3_TX_Trig_Ctrl.

Table 3–5: SPI3_TX_Trig_Ctrl group symbol table definitions

Symbol	Trig_Control group value TSOP TEOP TERR	Description
Any control	X X X	-
SOP	1 X X	Start of packet
EOP	X 1 X	End of packet
ERROR	X 1 1	Erroneous packet

Table 3–6 shows the definitions for the symbol, bit pattern, and meaning of the group symbols in the Parity symbol table for the SPI3_TX support package. The Parity symbol table file name SPI3_TX_Parity.

Table 3–6: SPI3_TX Parity group symbol table definitions

Symbol	Parity group value TPRTY	Description
Parity_0	0	Parity signal is low
Parity_1	1	Parity signal is high

The symbol table file for SPI3_RX support package is SPI3_RX_Ctrl.

Table 3–7: SPI3_RX_Ctrl group symbol table definitions

Symbol	Ctrl group value RSX RVAL RENB RSOP	REOP RERR RPRTY RMOD1	RMOD0	Description
DATA	0 1 X 0	0 X X X	X	Valid data on RDAT bus
SOP	0 1 X 1	0 X X X	X	Sample at which RSOP is asserted
PORT_ADDRESS	1 0 X 0	0 X X X	X	Physical port address

Table 3–7: SPI3_RX_Ctrl group symbol table definitions (Cont.)

Symbol	Ctrl group value RSX RVAL RENB RSOP REOP RERR RPRTY RMOD1 RMOD0	Description
EOP	0 1 X 0 1 0 X X X	Sample at which REOP is asserted
ERROR	0 1 X X 1 1 X X X	Erroneous packet received over RDAT bus
SOP&EOP	X 1 X 1 1 X X X X	Sample at which RSOP and REOP are asserted

***NOTE**. Binary values are displayed for those control group words that do not have any symbols assigned to them.*

Table 3–8 shows the definitions for the symbol, bit pattern, and meaning of the group symbols in the EasyTrigger symbol table for the SPI3_RX support package. The EasyTrigger symbol table file name SPI3_RX_Trig_Ctrl.

Table 3–8: SPI3_RX_Trig_Ctrl group symbol table definitions

Symbol	Trig_Control group value RSOP REOP RERR	Description
Any control	X X X	
SOP	1 X X	Start of packet
EOP	X 1 X	End of packet
ERROR	X 1 1	Erroneous packet

Table 3–9 shows the definitions for the symbol, bit pattern, and meaning of the group symbols in the Parity symbol table for the SPI3_RX support package. The Parity symbol table file name SPI3_RX_Parity.

Table 3–9: SPI3_RX Parity group symbol table definitions

Symbol	Parity group value	Description
	RPRTY	
Parity_0	0	Parity signal is low
Parity_1	1	Parity signal is high

Table 3–10 shows the definitions for the symbol, bit pattern, and meaning of the group symbols in the control symbol table for the SPI4 and SPI4_LVTTL support packages. The symbol table file for SPI4 and SPI4_LVTTL support packages is SPI4_Ctrl and SPI4_LVTTL_Ctrl. Use these symbols for triggering packet and control word information. By default, the group is off.

Table 3–10: SPI4_Ctrl/SPI4_LVTTL_Ctrl group symbol table definitions

Symbol	Ctrl group value	Description
	CTL_DM/CTL DAT15/DAT31 DAT14/DAT30 DAT13/DAT29 DAT12/DAT28	
(Any_Word)	1 X X X X	–
(Generic_SOP)	1 1 0 X 1	Packet start
(Generic_EOP)	1 X 1 X X	Packet end
(Generic_Abort)	1 X 0 1 X	Packet end abort
0: Idle, not_EOP, training_control	1 0 0 0 0	Training control word
1: Reserved	1 0 0 0 1	Reserved
2: Idle, Abort_last_packet	1 0 0 1 0	Idle control word, abort
3: Reserved	1 0 0 1 1	Reserved
4: Idle, EOP_with_2_bytes_valid	1 0 1 0 0	Idle control word, EOP, both the bytes valid
5: Reserved	1 0 1 0 1	Reserved
6: Idle, EOP_with_1_byte_valid	1 0 1 1 0	Idle control word, EOP, one byte valid
7: Reserved	1 0 1 1 1	Reserved
8: Valid, no_SOP, no_EOP	1 1 0 0 0	Valid packet, not SOP and EOP

Table 3–10: SPI4_Ctrl/SPI4_LVTTL_Ctrl group symbol table definitions (Cont.)

Symbol	Ctrl group value CTL_DM/CTL DAT15/DAT31 DAT14/DAT30 DAT13/DAT29	Ctrl group value DAT12/DAT28	Description
9: Valid, SOP, no_EOP	1 1 0 0	1	Valid packet, SOP and not EOP
A: Valid, no_SOP, abort	1 1 0 1	0	Valid packet, not SOP and abort
B: Valid, SOP, abort	1 1 0 1	1	Valid packet, SOP and abort
C: Valid, no_SOP, EOP_w/2_bytes_valid	1 1 1 0	0	Valid packet, not SOP and EOP with both the bytes valid
D: Valid, SOP, EOP_w/2_bytes_valid	1 1 1 0	1	Valid packet, SOP and EOP with both the bytes valid
E: Valid, no_SOP, EOP_w/1_byte_valid	1 1 1 1	0	Valid packet, not SOP and EOP with one byte valid
F: Valid, SOP, EOP_w/1_byte_valid	1 1 1 1	1	Valid packet, SOP and EOP with one byte valid

Information on basic operations describes how to use symbolic values for triggering and for displaying other channel groups symbolically.

Channel Assignment Tables

Channel assignments shown in Table 3–11 through Table 3–68 use the following conventions:

- All signals are required by the support package, unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB), descending to the least significant bit (LSB).
- Channel group assignments are for all modules, unless otherwise noted.
- Any SPI-3 signal ending with the letter “B” indicates that the signal is asserted low.

SPI3_TX Channel Group Assignments

Tables 3–11 through 3–18 show the channel assignments for the logic analyzer groups for the SPI3_TX support package and the bus signal to which each channel connects.

Table 3–11 shows the probe section and channel assignments for the Address group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–11: Address group assignments for SPI3_TX support package

Bit order	Logic analyzer channel	SPI-3 transmit signal name
1 (MSB)	C3:7	TADR1
0	C3:6	TADR0

Table 3–12 shows the probe section and channel assignments for the DAT group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–12: DAT group assignments for SPI3_TX support package

Bit order	Logic analyzer channel	SPI-3 transmit signal name
31 (MSB)	D1:7	TDAT31
30	D1:6	TDAT30
29	D1:5	TDAT29
28	D1:4	TDAT28
27	D1:3	TDAT27
26	D1:2	TDAT26
25	D1:1	TDAT25
24	D1:0	TDAT24
23	D0:7	TDAT23
22	D0:6	TDAT22
21	D0:5	TDAT21
20	D0:4	TDAT20
19	D0:3	TDAT19
18	D0:2	TDAT18
17	D0:1	TDAT17
16	D0:0	TDAT16
15	A1:7	TDAT15
14	A1:6	TDAT14
13	A1:5	TDAT13
12	A1:4	TDAT12

Table 3–12: DAT group assignments for SPI3_TX support package (Cont.)

Bit order	Logic analyzer channel	SPI-3 transmit signal name
11	A1:3	TDAT11
10	A1:2	TDAT10
9	A1:1	TDAT9
8	A1:0	TDAT8
7	A0:7	TDAT7
6	A0:6	TDAT6
5	A0:5	TDAT5
4	A0:4	TDAT4
3	A0:3	TDAT3
2	A0:2	TDAT2
1	A0:1	TDAT1
0 (LSB)	A0:0	TDAT0

Table 3–13 shows the probe section and channel assignments for the Control group and the bus signal to which each channel connects. By default, this channel group is displayed in symbols. The symbol table file name is SPI3_TX_Ctrl.

Table 3–13: Control group assignments for SPI3_TX support package

Bit order	Logic analyzer channel	SPI-3 transmit signal name
7 (MSB)	C2:3	TSX
6	C2:2	TENB
5	C2:0	TSOP
4	C2:1	TEOP
3	C3:1	TERR
2	C3:3	TPRTY
1	C3:5	TMOD1
0 (LSB)	C3:4	TMOD0

Table 3–14 shows the probe section and channel assignments for the DTPA group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–14: DTPA group assignments for SPI3_TX support package

Bit order	Logic analyzer channel	SPI-3 transmit signal name
3 (MSB)	C2:7	DTPA3
2	C2:6	DTPA2
1	C2:5	DTPA1
0 (LSB)	C2:4	DTPA0

Table 3–15 shows the probe section and channel assignments for the Misc group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–15: Misc group assignments for SPI3_TX support package

Bit order	Logic analyzer channel	SPI-3 transmit signal name
1 (MSB)	C3:2	PTPA
0	C3:0	STPA

Table 3–16 shows the probe section and channel assignments for the Trig_Control group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–16: Trig_Control group assignments for SPI3_TX support package

Bit order	Logic analyzer channel	SPI-3 transmit signal name
2 (MSB)	C2:0	TSOP
1	C2:1	TEOP
0 (LSB)	C3:1	TERR

Table 3–17 shows the probe section and channel assignments for the Trig_DAT[7:0] group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–17: Trig_DAT[7:0] group assignments for SPI3_TX support package

Bit order	Logic analyzer channel	SPI-3 transmit signal name
7 (MSB)	A0:7	TDAT7
6	A0:6	TDAT6
5	A0:5	TDAT5
4	A0:4	TDAT4
3	A0:3	TDAT3
2	A0:2	TDAT2
1	A0:1	TDAT1
0 (LSB)	A0:0	TDAT0

Table 3–18 shows the probe section and channel assignments for the Trig_DAT[31:0] group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–18: Trig_DAT[31:0] group assignments for SPI3_TX support package

Bit order	Logic analyzer channel	SPI-3 transmit signal name
31 (MSB)	D1:7	TDAT31
30	D1:6	TDAT30
29	D1:5	TDAT29
28	D1:4	TDAT28
27	D1:3	TDAT27
26	D1:2	TDAT26
25	D1:1	TDAT25
24	D1:0	TDAT24
23	D0:7	TDAT23
22	D0:6	TDAT22
21	D0:5	TDAT21
20	D0:4	TDAT20
19	D0:3	TDAT19
18	D0:2	TDAT18

Table 3–18: Trig_DAT[31:0] group assignments for SPI3_TX support package (Cont.)

Bit order	Logic analyzer channel	SPI-3 transmit signal name
17	D0:1	TDAT17
16	D0:0	TDAT16
15	A1:7	TDAT15
14	A1:6	TDAT14
13	A1:5	TDAT13
12	A1:4	TDAT12
11	A1:3	TDAT11
10	A1:2	TDAT10
9	A1:1	TDAT9
8	A1:0	TDAT8
7	A0:7	TDAT7
6	A0:6	TDAT6
5	A0:5	TDAT5
4	A0:4	TDAT4
3	A0:3	TDAT3
2	A0:2	TDAT2
1	A0:1	TDAT1
0 (LSB)	A0:0	TDAT0

SPI3_RX Channel Group Assignments

Tables 3–19 through 3–23 show the channel assignments for the logic analyzer groups for the SPI3_RX support package and the bus signal to which each channel connects.

Table 3–19 shows the probe section and channel assignments for the DAT group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–19: DAT group assignments for SPI3_RX support package

Bit order	Logic analyzer channel	SPI-3 receive signal name
31 (MSB)	D1:7	RDAT31
30	D1:6	RDAT30
29	D1:5	RDAT29
28	D1:4	RDAT28

Table 3–19: DAT group assignments for SPI3_RX support package (Cont.)

Bit order	Logic analyzer channel	SPI-3 receive signal name
27	D1:3	RDAT27
26	D1:2	RDAT26
25	D1:1	RDAT25
24	D1:0	RDAT24
23	D0:7	RDAT23
22	D0:6	RDAT22
21	D0:5	RDAT21
20	D0:4	RDAT20
19	D0:3	RDAT19
18	D0:2	RDAT18
17	D0:1	RDAT17
16	D0:0	RDAT16
15	A1:7	RDAT15
14	A1:6	RDAT14
13	A1:5	RDAT13
12	A1:4	RDAT12
11	A1:3	RDAT11
10	A1:2	RDAT10
9	A1:1	RDAT9
8	A1:0	RDAT8
7	A0:7	RDAT7
6	A0:6	RDAT6
5	A0:5	RDAT5
4	A0:4	RDAT4
3	A0:3	RDAT3
2	A0:2	RDAT2
1	A0:1	RDAT1
0 (LSB)	A0:0	RDAT0

Table 3–20 shows the probe section and channel assignments for the Control group and the bus signal to which each channel connects. By default, this channel group is displayed in symbols. The symbol table file name is SPI3_RX_Ctrl.

Table 3–20: Control group assignments for SPI3_RX support package

Bit order	Logic analyzer channel	SPI-3 receive signal name
8	C2:3	RSX
7	Clock:1	RVAL
6	C2:2	RENB
5	C2:0	RSOP
4	C2:1	REOP
3	C3:1	RERR
2	C3:3	RPRTY
1	C3:5	RMOD1
0 (LSB)	C3:4	RMOD0

Table 3–21 shows the probe section and channel assignments for the Trig_Control group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–21: Trig_Control group assignments for SPI3_RX support package

Bit order	Logic analyzer channel	SPI-3 transmit signal name
2 (MSB)	C2:0	RSOP
1	C2:1	REOP
0 (LSB)	C3:1	RERR

Table 3–22 shows the probe section and channel assignments for the Trig_DAT[7:0] group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–22: Trig_DAT[7:0] group assignments for SPI3_RX support package

Bit order	Logic analyzer channel	SPI-3 transmit signal name
7 (MSB)	A0:7	RDAT7
6	A0:6	RDAT6

Table 3–22: Trig_DAT[7:0] group assignments for SPI3_RX support package (Cont.)

Bit order	Logic analyzer channel	SPI-3 transmit signal name
5	A0:5	RDAT5
4	A0:4	RDAT4
3	A0:3	RDAT3
2	A0:2	RDAT2
1	A0:1	RDAT1
0 (LSB)	A0:0	RDAT0

Table 3–23 shows the probe section and channel assignments for the Trig_DAT[31:0] group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–23: Trig_DAT[31:0] group assignments for SPI3_RX support package

Bit order	Logic analyzer channel	SPI-3 transmit signal name
31 (MSB)	D1:7	RDAT31
30	D1:6	RDAT30
29	D1:5	RDAT29
28	D1:4	RDAT28
27	D1:3	RDAT27
26	D1:2	RDAT26
25	D1:1	RDAT25
24	D1:0	RDAT24
23	D0:7	RDAT23
22	D0:6	RDAT22
21	D0:5	RDAT21
20	D0:4	RDAT20
19	D0:3	RDAT19
18	D0:2	RDAT18
17	D0:1	RDAT17
16	D0:0	RDAT16
15	A1:7	RDAT15
14	A1:6	RDAT14

Table 3–23: Trig_DAT[31:0] group assignments for SPI3_RX support package (Cont.)

Bit order	Logic analyzer channel	SPI-3 transmit signal name
13	A1:5	RDAT13
12	A1:4	RDAT12
11	A1:3	RDAT11
10	A1:2	RDAT10
9	A1:1	RDAT9
8	A1:0	RDAT8
7	A0:7	RDAT7
6	A0:6	RDAT6
5	A0:5	RDAT5
4	A0:4	RDAT4
3	A0:3	RDAT3
2	A0:2	RDAT2
1	A0:1	RDAT1
0 (LSB)	A0:0	RDAT0

SPI4 and SPI4_LVTTL Channel Group Assignments

The SPI-4.2 supports are common to both the SPI-4.2 Transmit and Receive buses. Therefore:

- TDAT and RDAT are referred to as DAT
- TCTL and RCTL are referred to as CTL
- TSCLK and RSCLK are referred to as SCLK
- TDCLK and RDCLK are referred to as DCLK

When you use the SPI4 and SPI4_LVTTL supports, do not connect the following logic analyzer channels to any signals because they are demuxed.

Qual:0
D3:7-0
D1:7-0
C1:7
C1:6

Tables 3–24 through 3–49 show the channel assignments for the groups of the SPI4 and SPI4_LVTTL support packages and the bus signal to which each channel connects.

Table 3–24 shows the probe section and channel assignments for the $CTL group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–24: $CTL group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	Clock:1	CTL
0	Qual:0	CTL_DM

Table 3–25 shows the probe section and channel assignments for the $DAT0 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–25: $DAT0 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A3:0	DAT0
0	D3:0	DAT16

Table 3–26 shows the probe section and channel assignments for the $DAT1 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–26: $DAT1 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A3:1	DAT1
0	D3:1	DAT17

Table 3–27 shows the probe section and channel assignments for the $DAT2 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–27: $DAT2 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A3:2	DAT2
0	D3:2	DAT18

Table 3–28 shows the probe section and channel assignments for the $DAT3 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–28: $DAT3 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A3:3	DAT3
0	D3:3	DAT19

Table 3–29 shows the probe section and channel assignments for the $DAT4 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–29: $DAT4 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A3:4	DAT4
0	D3:4	DAT20

Table 3–30 shows the probe section and channel assignments for the $DAT5 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–30: $DAT5 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A3:5	DAT5
0	D3:5	DAT21

Table 3–31 shows the probe section and channel assignments for the $DAT6 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–31: $DAT6 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A3:6	DAT6
0	D3:6	DAT22

Table 3–32 shows the probe section and channel assignments for the $DAT7 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–32: $DAT7 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A3:7	DAT7
0	D3:7	DAT23

Table 3–33 shows the probe section and channel assignments for the $DAT8 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–33: $DAT8 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A1:0	DAT8
0	D1:0	DAT24

Table 3–34 shows the probe section and channel assignments for the $DAT9 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–34: $DAT9 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A1:1	DAT9
0	D1:1	DAT25

Table 3–35 shows the probe section and channel assignments for the $DAT10 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–35: $DAT10 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A1:2	DAT10
0	D1:2	DAT26

Table 3–36 shows the probe section and channel assignments for the $DAT11 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–36: $DAT11 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A1:3	DAT11
0	D1:3	DAT27

Table 3–37 shows the probe section and channel assignments for the $DAT12 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–37: $DAT12 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A1:4	DAT12
0	D1:4	DAT28

Table 3–38 shows the probe section and channel assignments for the $DAT13 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–38: $DAT13 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A1:5	DAT13
0	D1:5	DAT29

Table 3–39 shows the probe section and channel assignments for the $DAT14 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–39: $DAT14 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A1:6	DAT14
0	D1:6	DAT30

Table 3–40 shows the probe section and channel assignments for the $DAT15 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–40: $DAT15 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A1:7	DAT15
0	D1:7	DAT31

Table 3–41 shows the probe section and channel assignments for the $STAT0 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–41: $STAT0 group assignments for SPI4 support package

Bit order	Logic analyzer channel	SPI4 support package signal name
1 (MSB)	C3:6	STAT0
0	C1:6	STAT0_DM

Table 3–42 shows the probe section and channel assignments for the $STAT1 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–42: $STAT1 group assignments for SPI4 support package

Bit order	Logic analyzer channel	SPI4 support package signal name
1 (MSB)	C3:7	STAT1
0	C1:7	STAT1_DM

NOTE*. The groups $STAT0 and $STAT1 are used only in the SPI4 support package.*

Table 3–43 shows the probe section and channel assignments for the DATA group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–43: DATA group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
31 (MSB)	A1:7	DAT15
30	A1:6	DAT14
29	A1:5	DAT13
28	A1:4	DAT12
27	A1:3	DAT11
26	A1:2	DAT10

Table 3–43: DATA group assignments for SPI4 and SPI4_LVTTL support packages (Cont.)

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
25	A1:1	DAT9
24	A1:0	DAT8
23	A3:7	DAT7
22	A3:6	DAT6
21	A3:5	DAT5
20	A3:4	DAT4
19	A3:3	DAT3
18	A3:2	DAT2
17	A3:1	DAT1
16	A3:0	DAT0
15	D1:7	DAT31
14	D1:6	DAT30
13	D1:5	DAT29
12	D1:4	DAT28
11	D1:3	DAT27
10	D1:2	DAT26
9	D1:1	DAT25
8	D1:0	DAT24
7	D3:7	DAT23
6	D3:6	DAT22
5	D3:5	DAT21
4	D3:4	DAT20
3	D3:3	DAT19
2	D3:2	DAT18
1	D3:1	DAT17
0 (LSB)	D3:0	DAT16

Table 3–44 shows the probe section and channel assignments for the CTL[1:0] group and the bus signal to which each channel connects. By default, this channel group is displayed in binary.

Table 3–44: CTL[1:0] group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	Qual:0	CTL_DM
0	Clock:1	CTL

Table 3–45 shows the probe section and channel assignments for the STAT group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–45: STAT group channel assignments for SPI4 support package

Bit order	Logic analyzer channel	SPI4 support package signal name
3 (MSB)	C3:7	STAT1
2	C3:6	STAT0
1	C1:7	STAT1_DM
0 (LSB)	C1:6	STAT0_DM

Table 3–46 shows the probe section and channel assignments for the STAT group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–46: STAT group channel assignments for SPI4_LVTTL support package

Bit order	Logic analyzer channel	SPI4_LVTTL support package signal name
1 (MSB)	C3:7	STAT1
0	C3:6	STAT0

Table 3–47 shows the probe section and channel assignments for the STAT_A group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–47: STAT_A group channel assignments for SPI4 support package

Bit order	Logic analyzer channel	SPI4 support package signal name
1 (MSB)	C3:7	STAT1
0	C3:6	STAT0

Table 3–48 shows the probe section and channel assignments for the STAT_B group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–48: STAT_B group channel assignments for SPI4 support package

Bit order	Logic analyzer channel	SPI4 support package signal name
1	C1:7	STAT1_DM
0	C1:6	STAT0_DM

NOTE*. The groups STAT_A and $STAT_B are used only in the SPI4 support package.*

Table 3–49 shows the probe section and channel assignments for the SCLK group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–49: SCLK group channel assignments for SPI4_LVTTL support package

Bit order	Logic analyzer channel	SPI4_LVTTL support package signal name
1	Clock:3	SCLK

EasyTrigger Channel Assignments

Tables 3–50 through 3–58 show the EasyTrigger channel assignments for the groups and the bus signal to which each channel connects. These groups are common for both SPI4 and SPI4_LVTTL support packages.

Table 3–50 shows the probe section and channel assignments for the CTL_TYPE_A group and the bus signal to which each channel connects. By default, this channel group is off. The symbol tables SPI4_Ctrl and SPI4_LVTTL_Ctrl are associated with this group.

Table 3–50: CTL_TYPE_A group EasyTrigger channel assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
4 (MSB)	Clock:1	CTL
3	A1:7	DAT15
2	A1:6	DAT14
1	A1:5	DAT13
0 (LSB)	A1:4	DAT12

Table 3–51 shows the probe section and channel assignments for the CTL_TYPE_B group and the bus signal to which each channel connects. By default, this channel group is off. The symbol tables SPI4_Ctrl and SPI4_LVTTL_Ctrl are associated with this group.

Table 3–51: CTL_TYPE_B group EasyTrigger channel assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
4 (MSB)	Qual:0	CTL_DM
3	D1:7	DAT31
2	D1:6	DAT30
1	D1:5	DAT29
0 (LSB)	D1:4	DAT28

Table 3–52 shows the probe section and channel assignments for the CTL_TYPE_AB group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–52: CTL_TYPE_AB group EasyTrigger channel assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
9 (MSB)	Clock:1	CTL
8	A1:7	DAT15
7	A1:6	DAT14
6	A1:5	DAT13
5	A1:4	DAT12
4	Qual:0	CTL_DM
3	D1:7	DAT31
2	D1:6	DAT30
1	D1:5	DAT29
0 (LSB)	D1:4	DAT28

Table 3–53 shows the probe section and channel assignments for the DAT_PORT_A group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–53: DAT_PORT_A group EasyTrigger channel assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
7 (MSB)	A1:3	DAT11
6	A1:2	DAT10
5	A3:1	DAT9
4	A3:0	DAT8
3	A3:7	DAT7
2	A3:6	DAT6
1	A3:5	DAT5
0 (LSB)	A3:4	DAT4

Table 3–54 shows the probe section and channel assignments for the DAT_PORT_B group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–54: DAT_PORT_B group EasyTrigger channel assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
7 (MSB)	D1:3	DAT27
6	D1:2	DAT26
5	D1:1	DAT25
4	D1:0	DAT24
3	D3:7	DAT23
2	D3:6	DAT22
1	D3:5	DAT21
0 (LSB)	D3:4	DAT20

Table 3–55 shows the probe section and channel assignments for the DAT_AB group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–55: DAT_AB group EasyTrigger channel assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
31 (MSB)	A1:7	DAT15
30	A1:6	DAT14
29	A1:5	DAT13
28	A1:4	DAT12
27	A1:3	DAT11
26	A1:2	DAT10
25	A1:1	DAT9
24	A1:0	DAT8
23	A3:7	DAT7
22	A3:6	DAT6
21	A3:5	DAT5
20	A3:4	DAT4

Table 3–55: DAT_AB group EasyTrigger channel assignments for SPI4 and SPI4_LVTTL support packages (Cont.)

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
19	A3:3	DAT3
18	A3:2	DAT2
17	A3:1	DAT1
16	A3:0	DAT0
15	D1:7	DAT31
14	D1:6	DAT30
13	D1:5	DAT29
12	D1:4	DAT28
11	D1:3	DAT27
10	D1:2	DAT26
9	D1:1	DAT25
8	D1:0	DAT24
7	D3:7	DAT23
6	D3:6	DAT22
5	D3:5	DAT21
4	D3:4	DAT20
3	D3:3	DAT19
2	D3:2	DAT18
1	D3:1	DAT17
0 (LSB)	D3:0	DAT16

Table 3–56 shows the probe section and channel assignments for the DAT_BA group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–56: DAT_BA group EasyTrigger channel assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
31 (MSB)	D1:7	DAT31
30	D1:6	DAT30
29	D1:5	DAT29

Table 3–56: DAT_BA group EasyTrigger channel assignments for SPI4 and SPI4_LVTTL support packages (Cont.)

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
28	D1:4	DAT28
27	D1:3	DAT27
26	D1:2	DAT26
25	D1:1	DAT25
24	D1:0	DAT24
23	D3:7	DAT23
22	D3:6	DAT22
21	D3:5	DAT21
20	D3:4	DAT20
19	D3:3	DAT19
18	D3:2	DAT18
17	D3:1	DAT17
16	D3:0	DAT16
15	A1:7	DAT15
14	A1:6	DAT14
13	A1:5	DAT13
12	A1:4	DAT12
11	A1:3	DAT11
10	A1:2	DAT10
9	A1:1	DAT9
8	A1:0	DAT8
7	A3:7	DAT7
6	A3:6	DAT6
5	A3:5	DAT5
4	A3:4	DAT4
3	A3:3	DAT3
2	A3:2	DAT2
1	A3:1	DAT1
0 (LSB)	A3:0	DAT0

Table 3–57 shows the probe section and channel assignments for the DAT_A group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–57: DAT_A group channel EasyTrigger assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
15 (MSB)	A1:7	DAT15
14	A1:6	DAT14
13	A1:5	DAT13
12	A1:4	DAT12
11	A1:3	DAT11
10	A1:2	DAT10
9	A1:1	DAT9
8	A1:0	DAT8
7	A3:7	DAT7
6	A3:6	DAT6
5	A3:5	DAT5
4	A3:4	DAT4
3	A3:3	DAT3
2	A3:2	DAT2
1	A3:1	DAT1
0 (LSB)	A3:0	DAT0

Table 3–58 shows the probe section and channel assignments for the DAT_B group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3–58: DAT_B group EasyTrigger channel assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
15 (MSB)	D1:7	DAT31
14	D1:6	DAT30
13	D1:5	DAT29
12	D1:4	DAT28

Table 3–58: DAT_B group EasyTrigger channel assignments for SPI4 and SPI4_LVTTL support packages (Cont.)

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
11	D1:3	DAT27
10	D1:2	DAT26
9	D1:1	DAT25
8	D1:0	DAT24
7	D3:7	DAT23
6	D3:6	DAT22
5	D3:5	DAT21
4	D3:4	DAT20
3	D3:3	DAT19
2	D3:2	DAT18
1	D3:1	DAT17
0 (LSB)	D3:0	DAT16

Clock and Qualifier Channel Assignments

Tables 3–59 through 3–60 show the channel assignments for the clock and qualifier probes for the SPI3_TX interface, and the bus signal to which each channel connects.

Table 3–59: Clock channel assignments for SPI3_TX support package

Logic analyzer channel	SPI-3 transmit signal name
Clock:3	TFCLK

Table 3–60: Qualifier channel assignments for SPI3_TX support package

Logic analyzer channel	SPI-3 transmit signal name
C2:3	TSX
C2:2	TENB

Tables 3–61 through 3–62 show the channel assignments for the clock and qualifier probes for the SPI3_RX interface, and the bus signal to which each channel connects.

Table 3–61: Clock channel assignments for SPI3_RX support package

Logic analyzer channel	SPI-3 receive signal name
Clock:3	RFCLK

Table 3–62: Qualifier channel assignments for SPI3_RX support package

Logic analyzer channel	SPI-3 receive signal name
C2:3	RSX
C2:2	RENB
Clock:1	RVAL

Table 3–63 shows the channel assignments for the clock and qualifier probes for the SPI4 support, and the bus signal to which each channel connects.

Table 3–63: Clock and qualifier channel assignments for SPI4 support package

Logic analyzer channel	SPI4 support package signal name
Clock:0	DCLK

Table 3–64 shows the channel assignments for the clock and qualifier probes for the SPI4_LVTTL support, and the bus signal to which each channel connects.

Table 3–64: Clock and qualifier channel assignments for SPI4_LVTTL support package

Logic analyzer channel	SPI4_LVTTL support package signal name
Clock:0	DCLK
Clock:3	SCLK

Signals Required for Clocking and Disassembly

Tables 3–65 through 3–66 show the signals required for clocking and disassembly for the TCS101 product.

SPI-3 Signals. Tables 3–65 through 3–66 show the signals and logic analyzer channels required for clocking and disassembly of SPI3 transmit and receive interfaces.

Table 3–65: SPI-3 transmit signals required for clocking and disassembly

Logic analyzer channel	SPI-3 transmit signal/group name
Clock:3	TFCLK
C2:3-0, C3:1, C3:3, C3:4-5	Control group
A1, A0, D1, D0	DAT group
C2:7-4	DTPA group
C3:6-7	Address group
C3:2, C3:0	Misc

Table 3–66: SPI-3 receive signals required for clocking and disassembly

Logic analyzer channel	SPI-3 transmit signal/group name
Clock:3	RFCLK
C2:3-0, Clock:1, C3:1, C3:3, C3:4-5	Control group
A1, A0, D1, D0	DAT group

SPI-4.2 Signals. Tables 3–67 and 3–68 show the signals and logic analyzer channels required for clocking and disassembly of SPI4 and SPI4_LVTTL support packages.

Table 3–67: SPI-4.2 signals required for clocking and disassembly for SPI4 support package

Logic analyzer channel	SPI4 support package signal name
Clock:0	DCLK
Clock:1	CTL

Table 3–67: SPI-4.2 signals required for clocking and disassembly for SPI4 support package (Cont.)

Logic analyzer channel	SPI4 support package signal name
A1	DAT15-DAT8
A3	DAT7-DAT0
C3:7	STAT1
C3:6	STAT0

Table 3–68: SPI-4.2 signals required for clocking and disassembly for SPI4_LVTTL support package

Logic analyzer channel	SPI4_LVTTL support package signal name
Clock:0	DCLK
Clock:1	CTL
Clock:3	SCLK
A1	DAT15-DAT8
A3	DAT7-DAT0
C3:7	STAT1
C3:6	STAT0

Signal Source To Probe Connections

For design purposes, you may need to make connections between the Signal Source and the P6880 or the P6860 Logic Analyzer Probe. Refer to the *P6810, P6860, and P6880 Logic Analyzer Probes Instruction* manual, Tektronix part number 071-1059-XX, for more information on mechanical specifications. Tables 3–70 through 3–76 show the Signal Source to probe pin connections.

The recommended pin assignment is the AMP pin assignment for the SPI3_TX and SPI3_RX support packages. See Table 3–69.

Table 3–69: Recommended pin assignments for a Mictor connector (component side)

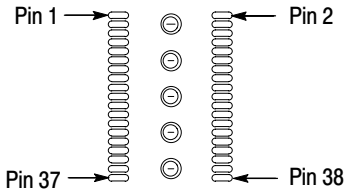
Type of pin assignment	Comments
Recommended  **AMP Pin Assignment**	Recommended. This pin assignment is the industry standard and is what we recommend that you use.

Figure 3–1 shows a sample of P6860 high density probe land footprint.

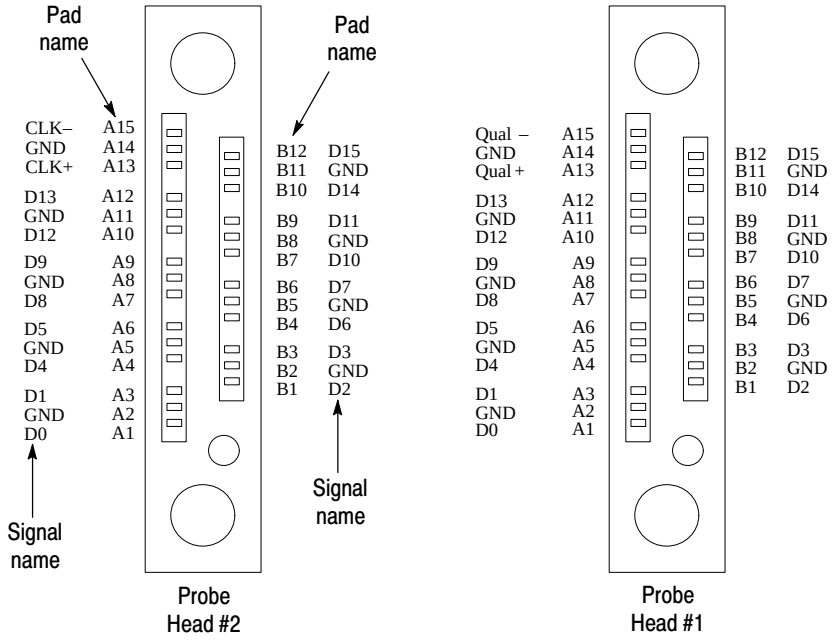


Figure 3–1: Sample of P6860 High-Density probe land footprint

Connections for SPI3_TX Support

Table 3–70 shows the pin connections for the SPI3_TX support package.

Table 3–70: Pin connections for SPI3_TX support package

Logic analyzer channel	SPI-3 signal name	P6860 pad name	P6860 probe signal name	AMP Mictor
Clock:3	TFCLK	A13	CK3+ Probe#1 probe head 2	Mictor 1 pin 5
–	–	A15*	CK3– Probe#1 probe head 2	–
C2:3	TSX	B3	Data3 Probe#1 probe head 2	Mictor 1 pin 31
C2:2	TENB	B1	Data2 Probe#1 probe head 2	Mictor 1 pin 33
C2:1	TEOP	A3	Data1 Probe#1 probe head 2	Mictor 1 pin 35
C2:0	TSOP	A1	Data0 Probe#1 probe head 2	Mictor 1 pin 37
C2:7	DTPA3	B6	Data7 Probe#1 probe head 2	Mictor 1 pin 23
C2:6	DTPA2	B4	Data6 Probe#1 probe head 2	Mictor 1 pin 25
C2:5	DTPA1	A6	Data5 Probe#1 probe head 2	Mictor 1 pin 27
C2:4	DTPA0	A4	Data4 Probe#1 probe head 2	Mictor 1 pin 29
C3:7	TADR1	B12	Data15 Probe#1 probe head 2	Mictor 1 pin 7

Table 3–70: Pin connections for SPI3_TX support package (Cont.)

Logic analyzer channel	SPI-3 signal name	P6860 pad name	P6860 probe signal name	AMP Mictor
C3:6	TADR0	B10	Data14 Probe#1 probe head 2	Mictor 1 pin 9
C3:5	TMOD1	A12	Data13 Probe#1 probe head 2	Mictor 1 pin 11
C3:4	TMOD0	A10	Data12 Probe#1 probe head 2	Mictor 1 pin 13
C3:3	TPRTY	B9	Data11 Probe#1 probe head 2	Mictor 1 pin 15
C3:2	PTPA	B7	Data10 Probe#1 probe head 2	Mictor 1 pin 17
C3:1	TERR	A9	Data9 Probe#1 probe head 2	Mictor 1 pin 19
C3:0	STPA	A7	Data8 Probe#1 probe head 2	Mictor 1 pin 21
D1:7	TDAT31	B12	Data15 Probe#2 probe head 1	Mictor 2 pin 7
D1:6	TDAT30	B10	Data14 Probe#2 probe head 1	Mictor 2 pin 9
D1:5	TDAT29	A12	Data13 Probe#2 probe head 1	Mictor 2 pin 11
D1:4	TDAT28	A10	Data12 Probe#2 probe head 1	Mictor 2 pin 13
D1:3	TDAT27	B9	Data11 Probe#2 probe head 1	Mictor 2 pin 15
D1:2	TDAT26	B7	Data10 Probe#2 probe head 1	Mictor 2 pin 17
D1:1	TDAT25	A9	Data9 Probe#2 probe head 1	Mictor 2 pin 19
D1:0	TDAT24	A7	Data8 Probe#2 probe head 1	Mictor 2 pin 21
D0:7	TDAT23	B6	Data7 Probe#2 probe head 1	Mictor 2 pin 23
D0:6	TDAT22	B4	Data6 Probe#2 probe head 1	Mictor 2 pin 25
D0:5	TDAT21	A6	Data5 Probe#2 probe head 1	Mictor 2 pin 27
D0:4	TDAT20	A4	Data4 Probe#2 probe head 1	Mictor 2 pin 29
D0:3	TDAT19	B3	Data3 Probe#2 probe head 1	Mictor 2 pin 31
D0:2	TDAT18	B1	Data2 Probe#2 probe head 1	Mictor 2 pin 33
D0:1	TDAT17	A3	Data1 Probe#2 probe head 1	Mictor 2 pin 35
D0:0	TDAT16	A1	Data0 Probe#2 probe head 1	Mictor 2 pin 37
A1:7	TDAT15	B12	Data15 Probe#2 probe head 2	Mictor 2 pin 8
A1:6	TDAT14	B10	Data14 Probe#2 probe head 2	Mictor 2 pin 10
A1:5	TDAT13	A12	Data13 Probe#2 probe head 2	Mictor 2 pin 12
A1:4	TDAT12	A10	Data12 Probe#2 probe head 2	Mictor 2 pin 14
A1:3	TDAT11	B9	Data11 Probe#2 probe head 2	Mictor 2 pin 16
A1:2	TDAT10	B7	Data10 Probe#2 probe head 2	Mictor 2 pin 18
A1:1	TDAT9	A9	Data9 Probe#2 probe head 2	Mictor 2 pin 20
A1:0	TDAT8	A7	Data8 Probe#2 probe head 2	Mictor 2 pin 22
A0:7	TDAT7	B6	Data7 Probe#2 probe head 2	Mictor 2 pin 24
A0:6	TDAT6	B4	Data6 Probe#2 probe head 2	Mictor 2 pin 26
A0:5	TDAT5	A6	Data5 Probe#2 probe head 2	Mictor 2 pin 28

Table 3–70: Pin connections for SPI3_TX support package (Cont.)

Logic analyzer channel	SPI-3 signal name	P6860 pad name	P6860 probe signal name	AMP Mictor
A0:4	TDAT4	A4	Data4 Probe#2 probe head 2	Mictor 2 pin 30
A0:3	TDAT3	B3	Data3 Probe#2 probe head 2	Mictor 2 pin 32
A0:2	TDAT2	B1	Data2 Probe#2 probe head 2	Mictor 2 pin 34
A0:1	TDAT1	A3	Data1 Probe#2 probe head 2	Mictor 2 pin 36
A0:0	TDAT0	A1	Data0 Probe#2 probe head 2	Mictor 2 pin 38

* **To be connected to ground in case of P6860 probe**

NOTE. *The logic analyzer module end of the P6434 probe cable has two parts (Pin 1 side and Pin 38 side). Connect the Pin 1 side of the module end to D1 and D0 sections of the logic analyzer module. Connect the Pin 38 side of the module end to A1 and A0 sections of the logic analyzer module.*

Refer to the P6434 Mass Termination Probe instruction manual, Tektronix part number 070-9793-03 to identify the Pin 1 side and the Pin 38 side of the AMP Mictor connector.

For example, the P6434 A probe's module end has two sections — Pin 1 side (A3-A2) and Pin 38 side (A1-A0). You should connect the A3-A2 side of the P6434 module end to D1-D0 of the logic analyzer module and A1-A0 side of the P6434 module end to A1-A0 of the logic analyzer module.

Connections for SPI3_RX Support

Table 3–71 shows the pin connections for the SPI3_RX support package.

Table 3–71: Pin connections for SPI3_RX support package

Logic analyzer channel	SPI-3 signal name	P6860 pad name	P6860 probe signal name	AMP Mictor
Clock:3	RFCLK	A13	CK3+ Probe#1 probe head 2	Mictor 1 pin 5
–	–	A15*	CK3– Probe#1 probe head 2	–
C2:3	RSX	B3	Data3 Probe#1 probe head 2	Mictor 1 pin 31
C2:2	RENB	B1	Data2 Probe#1 probe head 2	Mictor 1 pin 33
C2:1	REOP	A3	Data1 Probe#1 probe head 2	Mictor 1 pin 35
C2:0	RSOP	A1	Data0 Probe#1 probe head 2	Mictor 1 pin 37
C3:5	RMOD1	A12	Data13 Probe#1 probe head 2	Mictor 1 pin 11
C3:4	RMOD0	A10	Data12 Probe#1 probe head 2	Mictor 1 pin 13

Table 3–71: Pin connections for SPI3_RX support package (Cont.)

Logic analyzer channel	SPI-3 signal name	P6860 pad name	P6860 probe signal name	AMP Mictor
C3:3	RPRTY	B9	Data11 Probe#1 probe head 2	Mictor 1 pin 15
C3:1	RERR	A9	Data9 Probe#1 probe head 2	Mictor 1 pin 19
D1:7	RDAT31	B12	Data15 Probe#2 probe head 1	Mictor 2 pin 7
D1:6	RDAT30	B10	Data14 Probe#2 probe head 1	Mictor 2 pin 9
D1:5	RDAT29	A12	Data13 Probe#2 probe head 1	Mictor 2 pin 11
D1:4	RDAT28	A10	Data12 Probe#2 probe head 1	Mictor 2 pin 13
D1:3	RDAT27	B9	Data11 Probe#2 probe head 1	Mictor 2 pin 15
D1:2	RDAT26	B7	Data10 Probe#2 probe head 1	Mictor 2 pin 17
D1:1	RDAT25	A9	Data9 Probe#2 probe head 1	Mictor 2 pin 19
D1:0	RDAT24	A7	Data8 Probe#2 probe head 1	Mictor 2 pin 21
D0:7	RDAT23	B6	Data7 Probe#2 probe head 1	Mictor 2 pin 23
D0:6	RDAT22	B4	Data6 Probe#2 probe head 1	Mictor 2 pin 25
D0:5	RDAT21	A6	Data5 Probe#2 probe head 1	Mictor 2 pin 27
D0:4	RDAT20	A4	Data4 Probe#2 probe head 1	Mictor 2 pin 29
D0:3	RDAT19	B3	Data3 Probe#2 probe head 1	Mictor 2 pin 31
D0:2	RDAT18	B1	Data2 Probe#2 probe head 1	Mictor 2 pin 33
D0:1	RDAT17	A3	Data1 Probe#2 probe head 1	Mictor 2 pin 35
D0:0	RDAT16	A1	Data0 Probe#2 probe head 1	Mictor 2 pin 37
Clock:1	RVAL	A13	CK1+ Probe#2 probe head 2	Mictor 2 pin 6
–	–	A15*	CK1– Probe#2 probe head 2	–
A1:7	RDAT15	B12	Data15 Probe#2 probe head 2	Mictor 2 pin 8
A1:6	RDAT14	B10	Data14 Probe#2 probe head 2	Mictor 2 pin 10
A1:5	RDAT13	A12	Data13 Probe#2 probe head 2	Mictor 2 pin 12
A1:4	RDAT12	A10	Data12 Probe#2 probe head 2	Mictor 2 pin 14
A1:3	RDAT11	B9	Data11 Probe#2 probe head 2	Mictor 2 pin 16
A1:2	RDAT10	B7	Data10 Probe#2 probe head 2	Mictor 2 pin 18
A1:1	RDAT9	A9	Data9 Probe#2 probe head 2	Mictor 2 pin 20
A1:0	RDAT8	A7	Data8 Probe#2 probe head 2	Mictor 2 pin 22
A0:7	RDAT7	B6	Data7 Probe#2 probe head 2	Mictor 2 pin 24
A0:6	RDAT6	B4	Data6 Probe#2 probe head 2	Mictor 2 pin 26
A0:5	RDAT5	A6	Data5 Probe#2 probe head 2	Mictor 2 pin 28
A0:4	RDAT4	A4	Data4 Probe#2 probe head 2	Mictor 2 pin 30
A0:3	RDAT3	B3	Data3 Probe#2 probe head 2	Mictor 2 pin 32
A0:2	RDAT2	B1	Data2 Probe#2 probe head 2	Mictor 2 pin 34

Table 3–71: Pin connections for SPI3_RX support package (Cont.)

Logic analyzer channel	SPI-3 signal name	P6860 pad name	P6860 probe signal name	AMP Mictor
A0:1	RDAT1	A3	Data1 Probe#2 probe head 2	Mictor 2 pin 36
A0:0	RDAT0	A1	Data0 Probe#2 probe head 2	Mictor 2 pin 38

* **To be connected to ground in case of P6860 probe**

NOTE*. The logic analyzer module end of the P6434 probe cable has two parts (Pin 1 side and Pin 38 side). Connect the Pin 1 side of the module end to D1 and D0 sections of the logic analyzer module. Connect the Pin 38 side of the module end to A1 and A0 sections of the logic analyzer module.*

Refer to the P6434 Mass Termination Probe instruction manual, Tektronix part number 070-9793-03 to identify the Pin 1 side and the Pin 38 side of the AMP Mictor connector.

For example, the P6434 A probe's module end has two sections — Pin 1 side (A3-A2) and Pin 38 side (A1-A0). You should connect the A3-A2 side of the P6434 module end to D1-D0 of the logic analyzer module and A1-A0 side of the P6434 module end to A1-A0 of the logic analyzer module.

Connections for SPI4 and SPI4_LVTTL Supports

The SPI-4.2 supports are common to both the SPI-4.2 Transmit and Receive buses. Therefore:

- TDAT and RDAT are referred to as DAT
- TCTL and RCTL are referred to as CTL
- TSCLK and RSCLK are referred to as SCLK
- TDCLK and RDCLK are referred to as DCLK

When you use the SPI4 and SPI4_LVTTL supports, do not connect the following logic analyzer channels to any signals because they are demuxed.

Qual:0
D3:7-0
D1:7-0
C1:7
C1:6

Figure 3–2 shows a sample of P6880 differential probe land footprint.

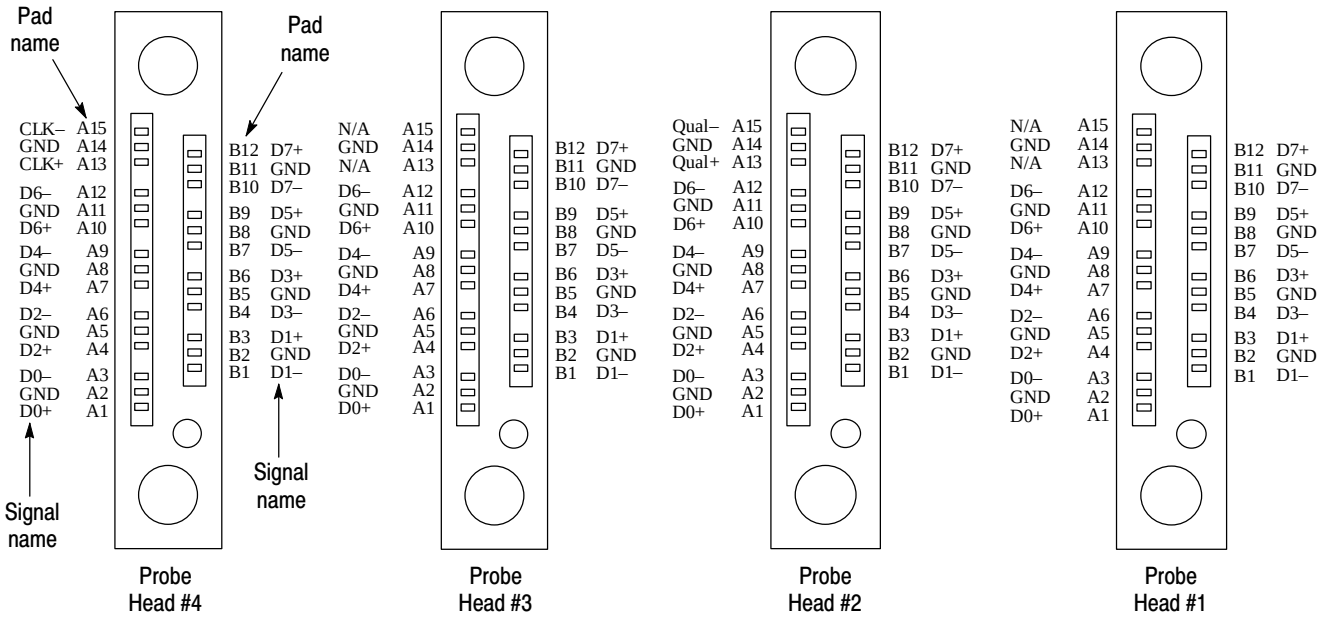


Figure 3–2: Sample of P6880 Differential probe land footprint

Tables 3–72 through 3–76 show the pin connections for the SPI4 and SPI4_LVTTL support packages.

NOTE*. The flow through the P6880 probe footprint has alternating polarities from channels. That is, the polarity changes between each signal pair: +/–, –/+, +/–, –/+ ensuring correct routing.*

The channel assignments are common for both Transmit and Receive interfaces.

Table 3–72: Pin connections for SPI4 and SPI4_LVTTL support packages (Probe#3)

Logic analyzer channel	P6880 probe signal name	P6880 probe #3 probe head 4	P6880 pad name	SPI-4.2 signal name
Clock:0	Clock:0–	CK:0–	A15	DCLK–
	Clock:0+	CK:0+	A13	DCLK+
A3:7	Data7+	A3:7+	B12	DAT7+
	Data7–	A3:7–	B10	DAT7–
A3:6	Data6–	A3:6–	A12	DAT6–

Table 3–72: Pin connections for SPI4 and SPI4_LVTTL support packages (Probe#3) (Cont.)

Logic analyzer channel	P6880 probe signal name	P6880 probe #3 probe head 4	P6880 pad name	SPI-4.2 signal name
	Data6+	A3:6+	A10	DAT6+
A3:5	Data5+	A3:5+	B9	DAT5+
	Data5–	A3:5–	B7	DAT5–
A3:4	Data4–	A3:4–	A9	DAT4–
	Data4+	A3:4+	A7	DAT4+
A3:3	Data3+	A3:3+	B6	DAT3+
	Data3–	A3:3–	B4	DAT3–
A3:2	Data2–	A3:2–	A6	DAT2–
	Data2+	A3:2+	A4	DAT2+
A3:1	Data1+	A3:1+	B3	DAT1+
	Data1–	A3:1–	B1	DAT1–
A3:0	Data0–	A3:0–	A3	DAT0–
	Data0+	A3:0+	A1	DAT0+

Table 3–73: Pin connections for SPI4 and SPI4_LVTTL support packages (Probe#2)

Logic analyzer channel	P6880 probe signal name	P6880 probe #2 probe head 4	P6880 pad name	SPI-4.2 signal name
Clock:1	Clock:1–	CK:1–	A15	CTL–
	Clock:1+	CK:1+	A13	CTL+
A1:7	Data7+	A1:7+	B12	DAT15+
	Data7–	A1:7–	B10	DAT15–
A1:6	Data6–	A1:6–	A12	DAT14–
	Data6+	A1:6+	A10	DAT14+
A1:5	Data5+	A1:5+	B9	DAT13+
	Data5–	A1:5–	B7	DAT13–
A1:4	Data4–	A1:4–	A9	DAT12–
	Data4+	A1:4+	A7	DAT12+
A1:3	Data3+	A1:3+	B6	DAT11+
	Data3–	A1:3–	B4	DAT11–
A1:2	Data2–	A1:2–	A6	DAT10–
	Data2+	A1:2+	A4	DAT10+
A1:1	Data1+	A1:1+	B3	DAT9+
	Data1–	A1:1–	B1	DAT9–

Table 3–73: Pin connections for SPI4 and SPI4_LVTTL support packages (Probe#2) (Cont.)

Logic analyzer channel	P6880 probe signal name	P6880 probe #2 probe head 4	P6880 pad name	SPI-4.2 signal name
A1:0	Data0–	A1:0–	A3	DAT8–
	Data0+	A1:0+	A1	DAT8+

If SCLK, STAT[1:0] are LVDS signals, use the channel assignments shown in Table 3–74 for the P6880 probe.

***NOTE**. For LVDS signals, the FIFO status clock (SCLK) is the same as DCLK.*

Table 3–74: Pin connections for SPI4 support package for FIFO Status LVDS signals (Probe#1)

Logic analyzer channel	P6880 probe signal name	P6880 probe #1 probe head 4	P6880 pad name	SPI-4.2 signal name
C3:7	Data7+	C3:7+	B12	STAT1+
	Data7–	C3:7–	B10	STAT1–
C3:6	Data6–	C3:6–	A12	STAT0–
	Data6+	C3:6+	A10	STAT0+

If SCLK, STAT[1:0] are LVTTL signals, use the channel assignments shown in Table 3–75 for the P6880 probe.

Table 3–75: Pin connections for SPI4_LVTTL support package for FIFO Status LVTTL signals (P6880)

Logic analyzer channel	P6880 probe signal name	P6880 probe #1 probe head 4	P6880 pad name	SPI-4.2 signal name
Clock:3	Clock:3–	CK3–	A15	GND
	Clock:3+	CK3+	A13	SCLK
C3:7	Data7+	C3:7+	B12	STAT1
	Data7–	C3:7–	B10	GND
C3:6	Data6–	C3:6–	A12	GND
	Data6+	C3:6+	A10	STAT0

If SCLK, STAT[1:0] are LVTTL signals, use the channel assignments shown in Table 3–76 for the P6860 probe.

Table 3–76: Pin connections for SPI4_LVTTL support package for FIFO Status LVTTL signals (P6860)

Logic analyzer channel	P6860 probe signal name	P6860 probe #1 probe head 2	P6860 pad name	SPI-4.2 support signal name
Clock:3	Clock:3–	CK3–	A15	GND
	Clock:3+	CK3+	A13	SCLK
C3:7	Data15	C3:7	B12	STAT1
C3:6	Data14	C3:6	B10	STAT0